Exhibit 1

Appl. No.: 10/002,461
Applicant(s): Keith R. Slavin
Filed: November 1, 2001
Title: LOW POWER, HASH-CONTENT ADDRESSABLE MEMORY ARCHITECTURE
Art Unit: 2189
Examiner: Reba I. Elmore

Docket No.: DB000955-000

DECLARATION UNDER RULE 131

I, Russel D. Slifer, state as follows:

1. I am Chief Patent Counsel for and authorized representative of Micron Technology, Inc., the assignee of the 10/002,461 application ("the '461 application").

2. In connection with the '461 application, an Invention Disclosure form identifying Keith R. Slavin as the inventor was submitted to the Micron patent department. A copy of the first and last pages of the Invention Disclosure form are attached as Exhibits A and B, respectively.

3. Attached to the Invention Disclosure form were four figures, attached hereto as Exhibit C. The figures of Exhibit C were read and understood by a witness, who signed and dated the figures on June 27, 2001.

4. I have reviewed and am familiar with the '461 application.

- The Figure on Sheet 1 of Exhibit C corresponds to Figure 1 of the '461 application.
- The Figure on Sheet 2 of Exhibit C corresponds to Figure 2 of the '461 application.
- The Figures on Sheets 3 and 4 of Exhibit C correspond to Figure 3 of the '461 application.

5. Independent claim 1 of the '461 application recites:

> inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of said input word;
> outputting a hash signal from each hash circuit;
> enabling portions of a CAM in response to said hash signals;
> inputting said input word to said CAM;
> comparing said input word in the enabled portions of said CAM; and
> outputting information responsive to said comparing.

6. Claim 1 reads on, for example, the Figure on Sheet 1 of Exhibit C and Figure 1 of the '461 application.

7 Independent claim 8 recites:

hashing a comparand word;
precharging certain portions of a CAM in response to said hashing; and
inputting said comparand word to said CAM.

8. Claim 8 reads on, for example, the Figure on Sheet 1 of Exhibit C and Figure 1 of the '461 application.

9. Independent claims 15 and 22 are method claims similar to claims 1 and 8, respectively. Claims 15 and 22 recite many of the same limitations of claims 1 and 8 respectively, utilizing the same physical elements outlined in those claims.

10. Independent claim 28 of the '461 application recites:

a CAM for receiving a comparand word;
a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word; and
a circuit, responsive to said hash signals, for precharging portions of said CAM.

11. Claim 28 reads on, for example, the Figure on Sheet 1 of Exhibit C and Figure 1 of the '461 application.

12. Claim 34 of the '461 application recites:

a CAM;
a plurality of hash circuits each for producing a hash signal in response to a portion of a comparand word;
a plurality of memory devices responsive to said hash circuits;
enable logic, responsive to said plurality of memory devices, for enabling portions of said CAM; and
a delay circuit for inputting the comparand word to said CAM.

13. The CAM, the plurality of hash circuits, the enable logic, and the delay circuit read on, for example, the Figure on Sheet 1 of Exhibit C and Figure 1 of the '461 application.

14. Independent claim 41 is a method claim reciting a method for initializing the hardware shown in the Figure on Sheet 1 of Exhibit C and Figure 1 of the '461 application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Russel D. Slifer 7/17/06
Date

Slifer - Exhibit A

INVENTION DISCLOSURE

1. **INVENTOR(S):**

2. Keith R Slavin

3. **DESCRIPTION:**

- **Title:**

A Low Power Hash-Ternary Contents-Addressable Memory

- **Brief Description:**

A Ternary Contents-Addressable-Memory (TCAM) normally consumes a lot of power because of simultaneous activity on large numbers of match lines - one for each TCAM entry. This patent shows how this activity can be reduced in a guaranteed fashion for any random or systematically generated set of TCAM entries by using a form of hardware based hashing. An example is shown for 128-bit IPv6 internet address matching used in routers. The power savings increase as TCAMs get larger. Micron can use this patent to build TCAMs with unrivaled worst-case power consumption.

4. **CONCEPTION & DOCUMENTATION OF INVENTION:**

- **Date when first conceived:**

Redacted

- **To whom was the idea first described:**

Redacted

- **On what date:**

Redacted

- **Date of the first tangible record:**

Redacted

- **Type and location:**

Redacted

5. **INFORMATION RELATED TO INVENTION:**

- **Related invention disclosures:**

Redacted

Slifer - Exhibit B

Redacted

8. **INVENTORS:**

Name : Keith R Slavin

Home Address : 8474 SW Chevy PLace

City : Beaverton **State** : OR **Zipcode** : 97008

Citizenship : U.S.A

Company : Micron Technology, Inc.

Work Phone # : 503 643 1182 **Mail Stop** : 831

Dept Name : SJDC CA-ARCH-ADV DEV **Dept #** : 402

Supervisor : Robert H. Mullis

Signature : Keith Slavin **Date** : 27th June, 2001

27th June, 2001

Slifer-Exhibit C 1/4

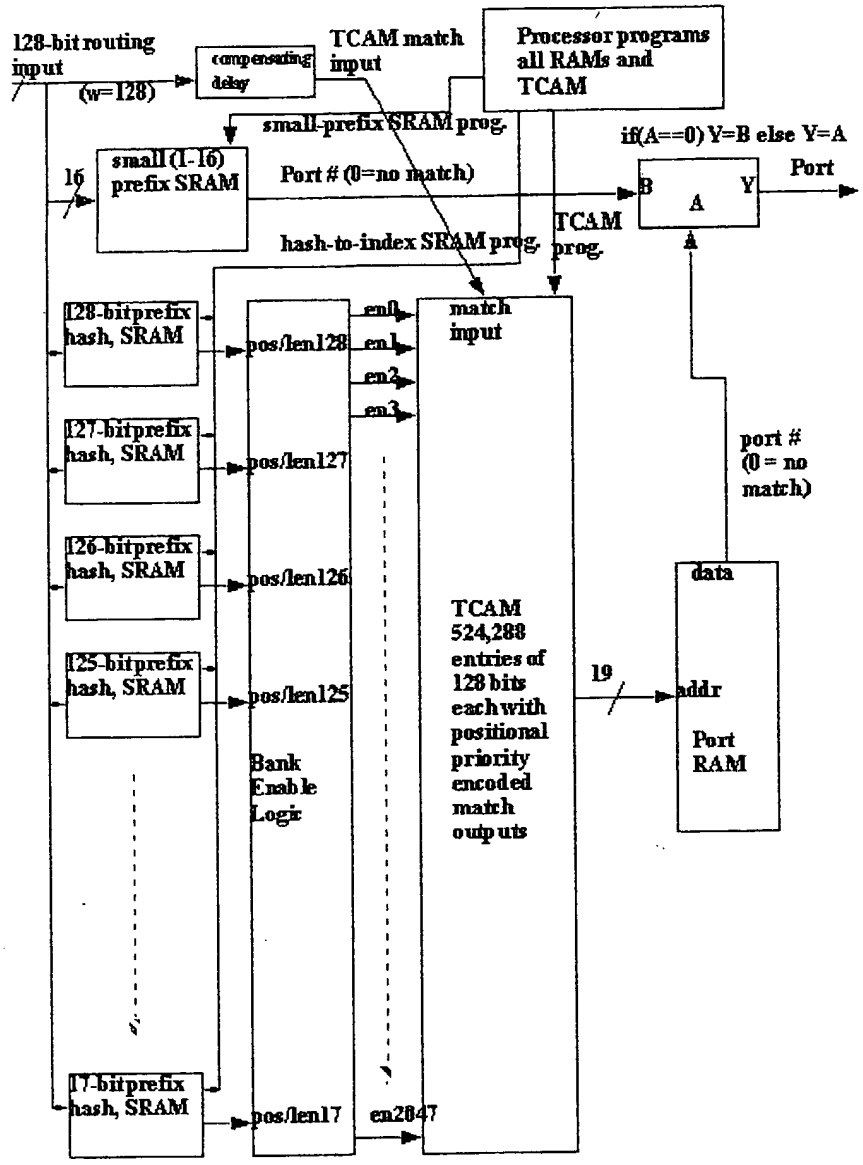

Figure 1. Block Diagram of Hash CAM System

Read & understood, [signature] 6/27/2001

Slifer-Exhibit C 2/4

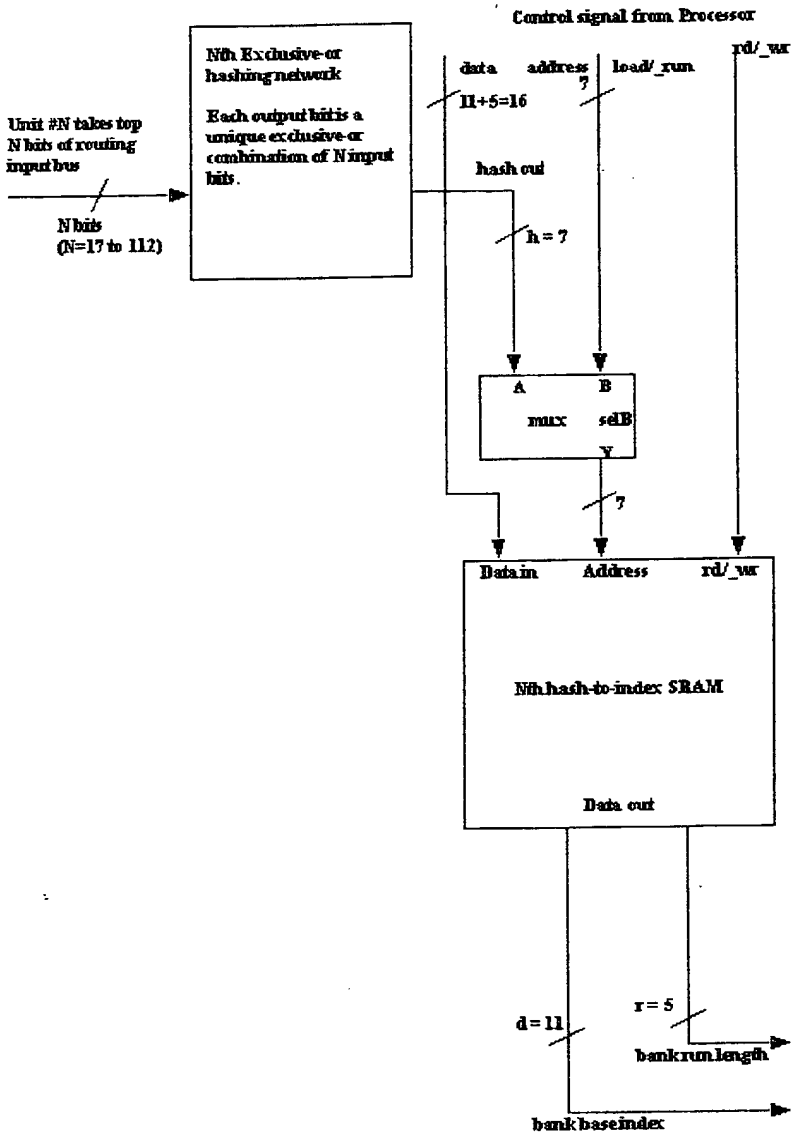

Figure 2: Block Diagram of a Hash, SRAM (112 instances from Figure 1)

Read & Understood. S Slifer 6/27/2001

Slifer-Exhibit C 3/4

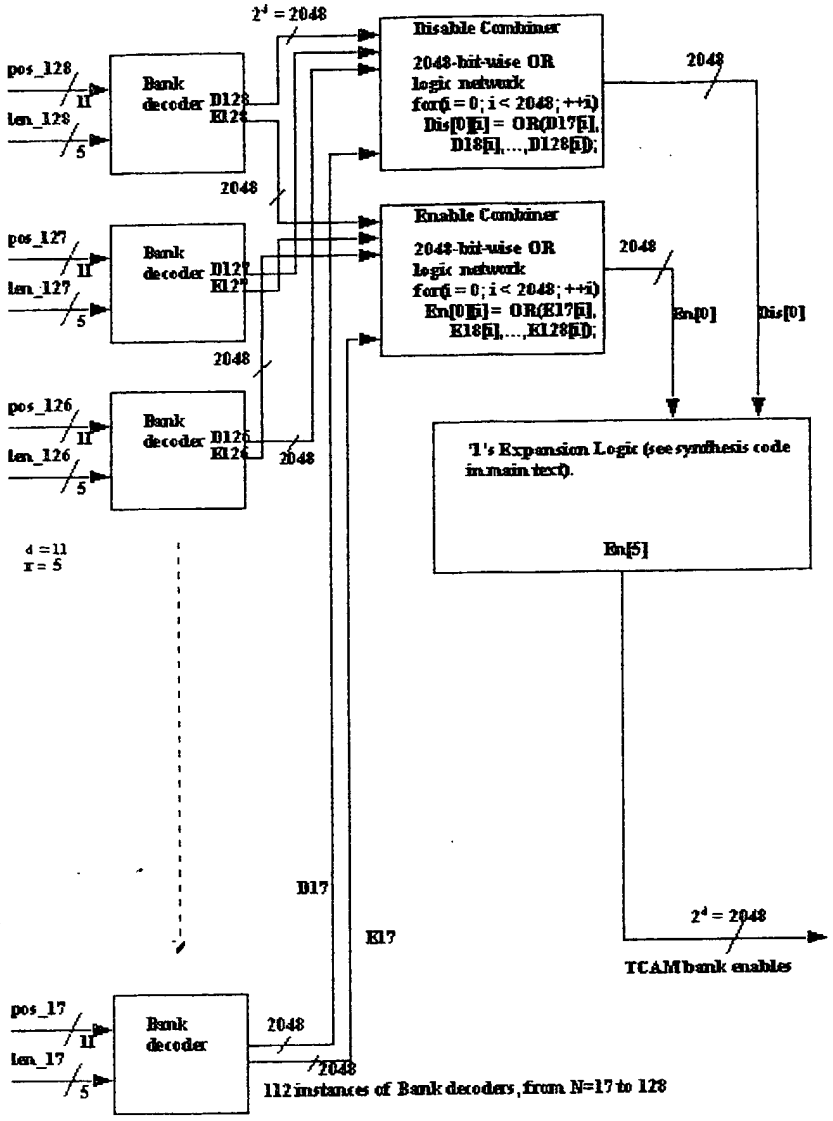

Figure 3: Bank Enable Logic Detail from Figure 1.

Read & understood, Shumm 6/27/2001

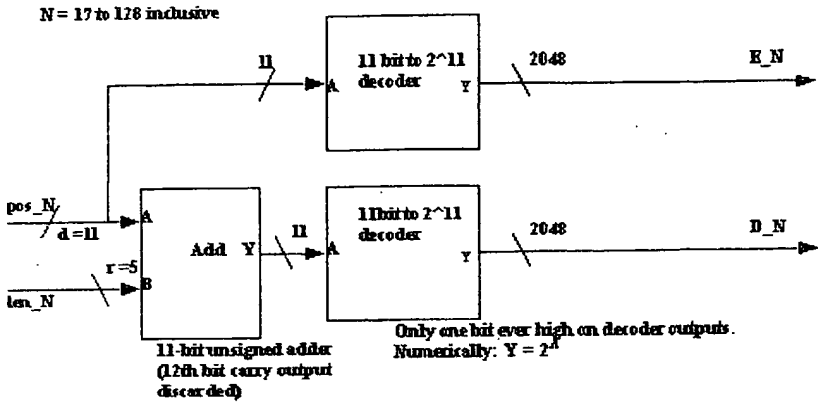

Figure 4: Bank Decoder Logic (112 instances from Figure 3)

Kent E. Weinstock 6/27/2001